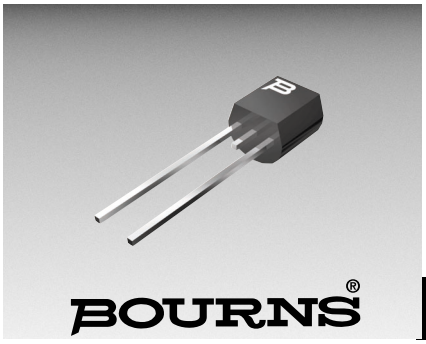

BOURNS®

TISP4070H3LM THRU TISP4115H3LM, TISP4125H3LM THRU TISP4220H3LM, TISP4240H3LM THRU TISP4400H3LM

BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

TISP4xxxH3LM Overvoltage Protector Series

TISP4xxxH3LM Overview

This TISP® device series protects central office, access and customer premise equipment against overvoltages on the telecom line. The TISP4xxxH3LM is available in a wide range of voltages and has a high current capability, allowing minimal series resistance to be used. These protectors have been specified mindful of the following standards and recommendations: GR-1089-CORE, FCC Part 68, UL1950, EN 60950, IEC 60950, ITU-T K.20, K.21 and K.45. The TISP4350H3LM meets the FCC Part 68 "B" ringer voltage requirement and survives the Type A and B impulse tests. These devices are housed in a through-hole DO-92 package (TO-92 package with cropped center leg).

Summary Electrical Characteristics

Part #	V_{DRM} V	$V_{(BO)}$ V	V_T @ I_T V	I_{DRM} µA	$I_{(BO)}$ mA	I_T A	I_H mA	C_o @ -2 V pF	Functionally Replaces
TISP4070H3	58	70	3	5	600	5	150	120	P0640EC†
TISP4080H3	65	80	3	5	600	5	150	120	P0720EC†
TISP4095H3	75	95	3	5	600	5	150	120	P0900EC†
TISP4115H3	90	115	3	5	600	5	150	120	P1100EC†
TISP4125H3	100	125	3	5	600	5	150	65	
TISP4145H3	120	145	3	5	600	5	150	65	P1300EC†
TISP4165H3	135	165	3	5	600	5	150	65	
TISP4180H3	145	180	3	5	600	5	150	65	P1500EC
TISP4220H3	160	220	3	5	600	5	150	65	P1800EC
TISP4240H3	180	240	3	5	600	5	150	55	
TISP4250H3	190	250	3	5	600	5	150	55	P2300EC†
TISP4260H3	200	260	3	5	600	5	150	55	
TISP4290H3	220	290	3	5	600	5	150	55	P2600EC†
TISP4300H3	230	300	3	5	600	5	150	55	
TISP4350H3	275	350	3	5	600	5	150	55	P3100EC
TISP4395H3	320	395	3	5	600	5	150	55	P3500EC†
TISP4400H3	300	400	3	5	600	5	150	55	

† Bourns part has an improved protection voltage

Summary Current Ratings

Parameter	I_{TSP} A						I_{TSM} A	di/dt A/µs
Waveshape	2/10	1.2/50, 8/20	10/160	5/320	10/560	10/1000	1 cycle 60 Hz	2/10 Wavefront
Value	500	300	250	200	160	100	60	400

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ITU-T K.20/21 Rating.....8 kV 10/700, 200 A 5/310

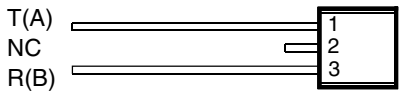
Ion-Implanted Breakdown Region
Precise and Stable Voltage
Low Voltage Overshoot under Surge

Device	V_{DRM} V	$V_{(BO)}$ V
'4070	58	70
'4080	65	80
'4095	75	95
'4115	90	115
'4125	100	125
'4145	120	145
'4165	135	165
'4180	145	180
'4220	160	220
'4240	180	240
'4250	190	250
'4260	200	260
'4290	220	290
'4300	230	300
'4350	275	350
'4395	320	395
'4400	300	400

Rated for International Surge Wave Shapes

Waveshape	Standard	I_{TSP} A
2/10 µs	GR-1089-CORE	500
8/20 µs	IEC 61000-4-5	300
10/160 µs	FCC Part 68	250
10/700 µs	ITU-T K.20/21	200
10/560 µs	FCC Part 68	160
10/1000 µs	GR-1089-CORE	100

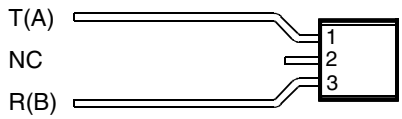
LM Package (Top View)



MD4XAT

NC - No internal connection on pin 2

LMF Package (LM Package with Formed Leads) (Top View)



MD4XAKB

NC - No internal connection on pin 2

Device Symbol

SD4XAA

Terminals T and R correspond to the alternative line designators of A and B

Low Differential Capacitance .....80 pF max.

..... UL Recognized Component

Description

These devices are designed to limit overvoltages on the telephone line. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. A single device provides 2-point protection and is typically used for the protection of 2-wire telecommunication equipment (e.g. between the Ring and Tip wires for telephones and modems). Combinations of devices can be used for multi-point protection (e.g. 3-point protection between Ring, Tip and Ground).

The protector consists of a symmetrical voltage-triggered bidirectional thyristor. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides.

How To Order

Device	Package	Carrier	Order As
TISP4xxxH3LM	Straight Lead DO-92 (LM)	Bulk Pack	TISP4xxxH3LM
		Tape and Reeled	TISP4xxxH3LMR
	Formed Lead DO-92 (LMF)	Tape and Reeled	TISP4xxxH3LMFR

Insert xxx value corresponding to protection voltages of 070, 080, 095, 115 etc.

Description (continued)

This TISP4xxxH3LM range consists of seventeen voltage variants to meet various maximum system voltage levels (58 V to 320 V). They are guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. These protection devices are supplied in a DO-92 (LM) cylindrical plastic package. The TISP4xxxH3LM is a straight lead DO-92 supplied in bulk pack and on tape and reel. The TISP4xxxH3LMF is a formed lead DO-92 supplied only on tape and reel. For lower rated impulse currents in the DO-92 package, the 50 A 10/1000 TISP4xxxM3LM series is available.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 1)	'4070	V_{DRM}	± 58	V
	'4080		± 65	
	'4095		± 75	
	'4115		± 90	
	'4125		±100	
	'4145		±120	
	'4165		±135	
	'4180		±145	
	'4220		±160	
	'4240		±180	
	'4250		±190	
	'4260		±200	
	'4290		±220	
	'4300		±230	
	'4350		±275	
	'4395		±320	
	'4400		±300	
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4)				
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)		I_{TSP}	500	A
8/20 µs (IEC 61000-4-5, combination wave generator, 1.2/50 voltage, 8/20 current)			300	
10/160 µs (FCC Part 68, 10/160 µs voltage wave shape)			250	
5/200 µs (VDE 0433, 10/700 µs voltage wave shape)			220	
0.2/310 µs (I 31-24, 0.5/700 µs voltage wave shape)			200	
5/310 µs (ITU-T K20/21, 10/700 µs voltage wave shape)			200	
5/310 µs (FTZ R12, 10/700 µs voltage wave shape)			200	
5/320 µs (FCC Part 68, 9/720 µs voltage wave shape)			200	
10/560 µs (FCC Part 68, 10/560 µs voltage wave shape)			160	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)			100	
Non-repetitive peak on-state current (see Notes 2, 3 and 5)				
20 ms (50 Hz) full sine wave		I_{TSM}	55	A
16.7 ms (60 Hz) full sine wave			60	
1000 s 50 Hz/60 Hz a.c.			2.3	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 100 A		di_T/dt	400	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. See Applications Information and Figure 10 for voltage values at lower temperatures.
2. Initially, the TISP4xxxH3LM must be in thermal equilibrium with T_J = 25 °C.
3. The surge may be repeated after the TISP4xxxH3LM returns to its initial conditions.
4. See Applications Information and Figure 11 for current ratings at other temperatures.
5. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 8 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

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Electrical Characteristics T_A= 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = \pm V_{DRM}$	T_A = 25 °C			±5	µA
			T_A = 85 °C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω	'4070			±70	V
			'4080			±80	
			'4095			±95	
			'4115			±115	
			'4125			±125	
			'4145			±145	
			'4165			±165	
			'4180			±180	
			'4220			±220	
			'4240			±240	
			'4250			±250	
			'4260			±260	
			'4290			±290	
			'4300			±300	
			'4350			±350	
			'4395			±395	
			'4400			±400	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000V/µs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'4070			±78	V
			'4080			±88	
			'4095			±103	
			'4115			±124	
			'4125			±134	
			'4145			±154	
			'4165			±174	
			'4180			±189	
			'4220			±230	
			'4240			±250	
			'4250			±261	
			'4260			±271	
			'4290			±301	
			'4300			±311	
			'4350			±362	
			'4395			±408	
			'4400			±413	
$I_{(BO)}$	Breakover current	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω		±0.15		±0.6	A
V_T	On-state voltage	I_T = ±5 A, t_W = 100 µs				±3	V
I_H	Holding current	I_T = ±5 A, di/dt = -/+30 mA/ms		±0.15		±0.6	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V	T_A = 85 °C			±10	µA

Electrical Characteristics T_A= 25 °C (Unless Otherwise Noted) (continued)

Parameter		Test Conditions		Min	Typ	Max	Unit
C_{off}	Off-state capacitance	f = 100 kHz, V_d = 1 V rms, V_D = 0,	4070 thru ‘4115		172	218	pF
			‘4125 thru ‘4220		95	120	
			‘4240 thru ‘4400		92	115	
		f = 100 kHz, V_d = 1 V rms, V_D = -1 V	‘4070 thru ‘4115		157	200	
			‘4125 thru ‘4220		85	110	
			‘4240 thru ‘4400		80	100	
		f = 100 kHz, V_d = 1 V rms, V_D = -2 V	‘4070 thru ‘4115		145	185	
			‘4125 thru ‘4220		78	100	
			‘4240 thru ‘4400		72	90	
		f = 100 kHz, V_d = 1 V rms, V_D = -50 V	‘4070 thru ‘4115		70	90	
			‘4125 thru ‘4220		33	43	
			‘4240 thru ‘4400		28	35	
		f = 100 kHz, V_d = 1 V rms, V_D = -100 V	‘4125 thru ‘4220		25	33	
		(see Note 6)	‘4240 thru ‘4400		22	28	

NOTE 6: To avoid possible voltage clipping, the ‘4125 is tested with V_D = -98 V.

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 7)			105	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C		55		

NOTE 7: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

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Parameter Measurement Information

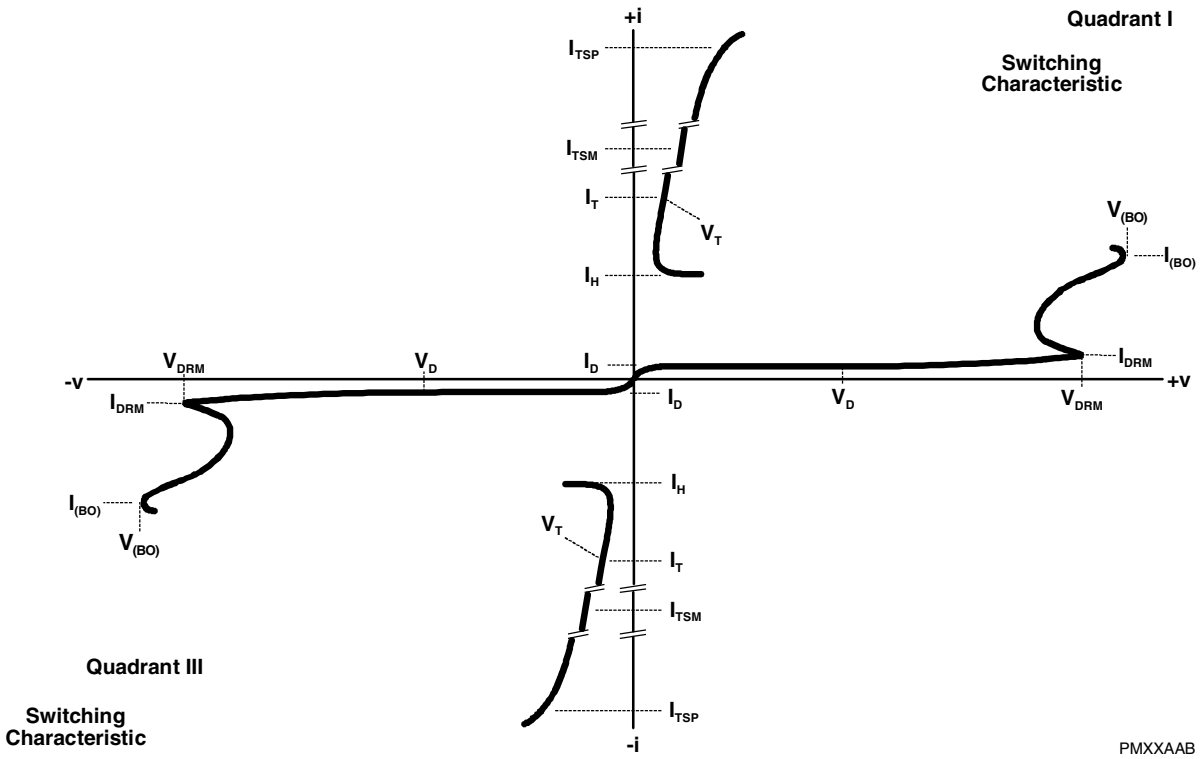

Figure 1. Voltage-current Characteristic for T and R Terminals
All Measurements are Referenced to the R Terminal

Typical Characteristics

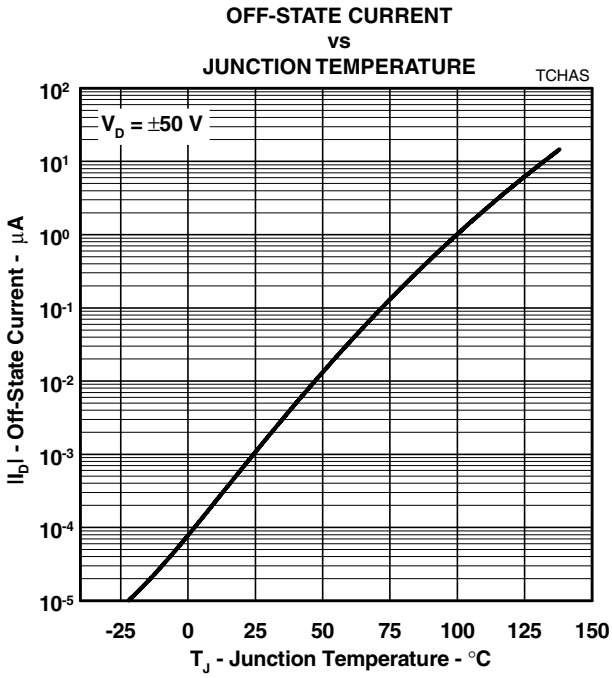

Figure 2.

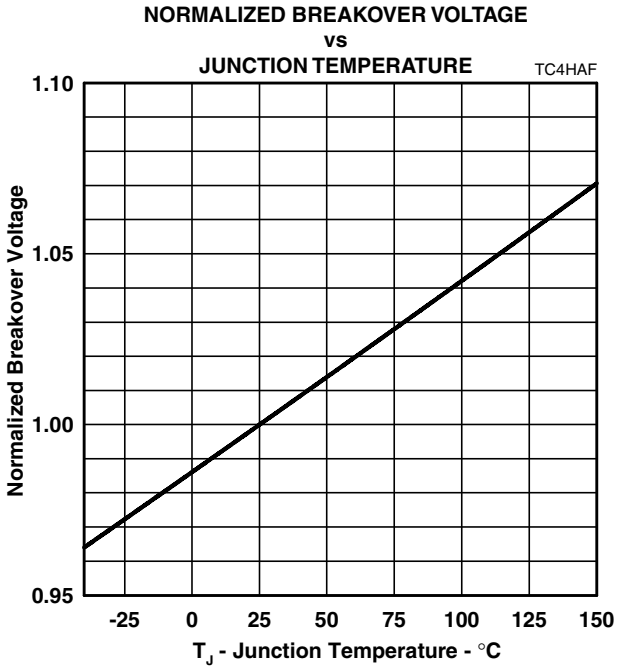

Figure 3.

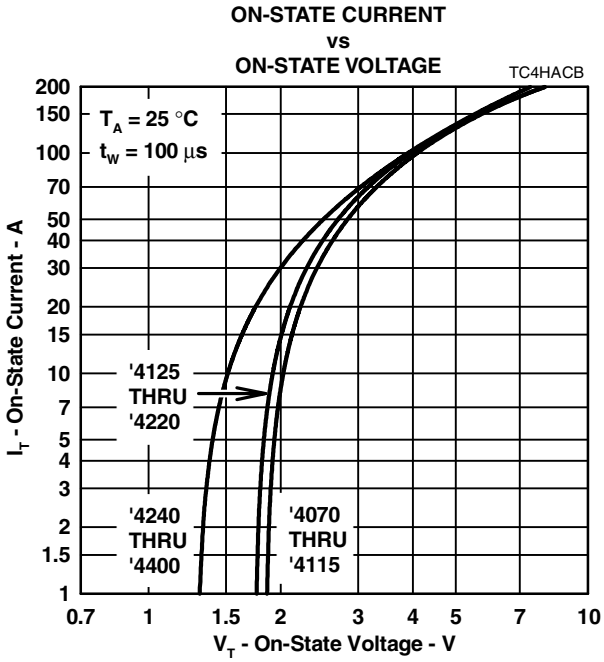

Figure 4.

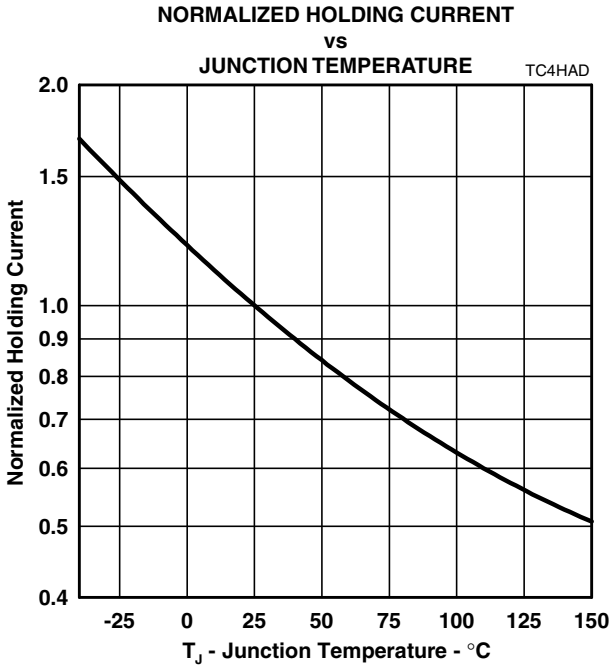

Figure 5.

Typical Characteristics

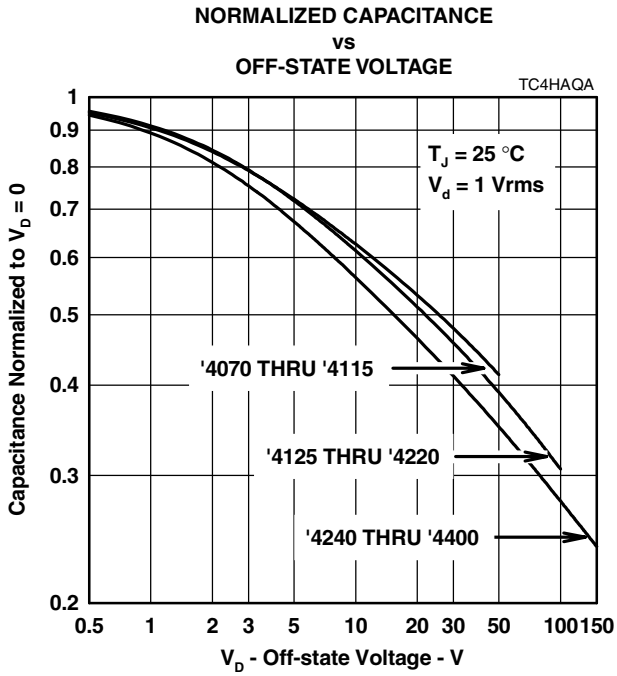

Figure 6.

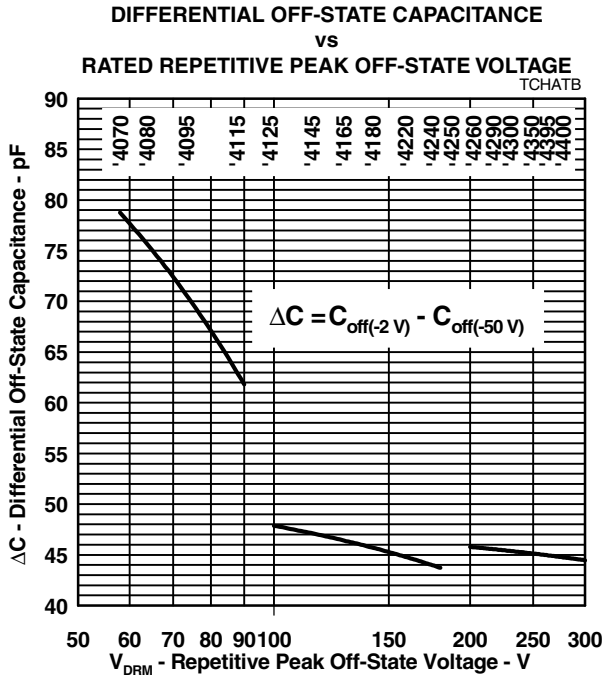

Figure 7.

Rating and Thermal Information

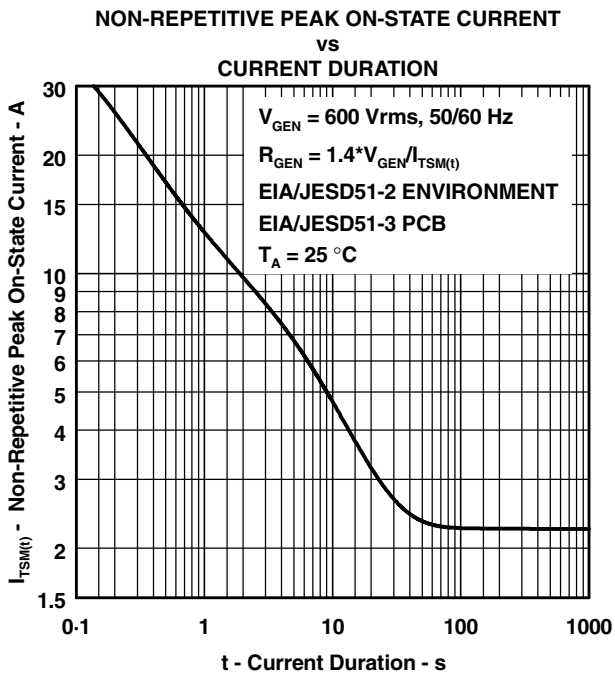

Figure 8.

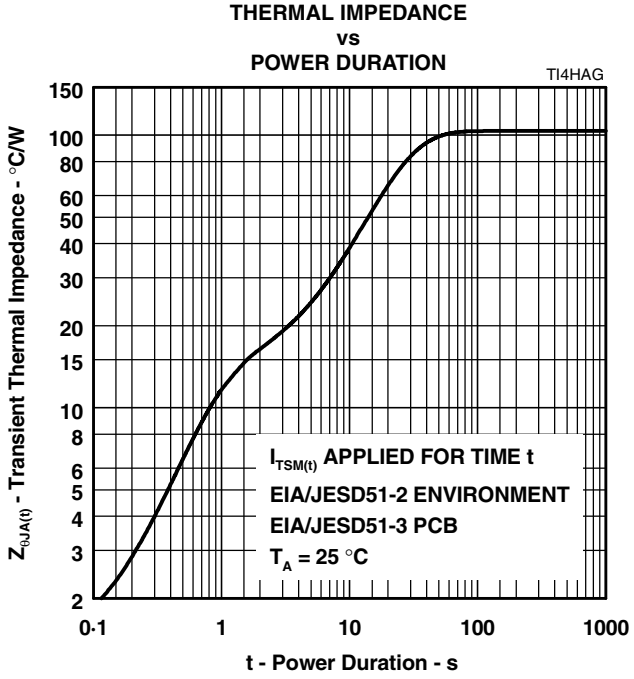

Figure 9.

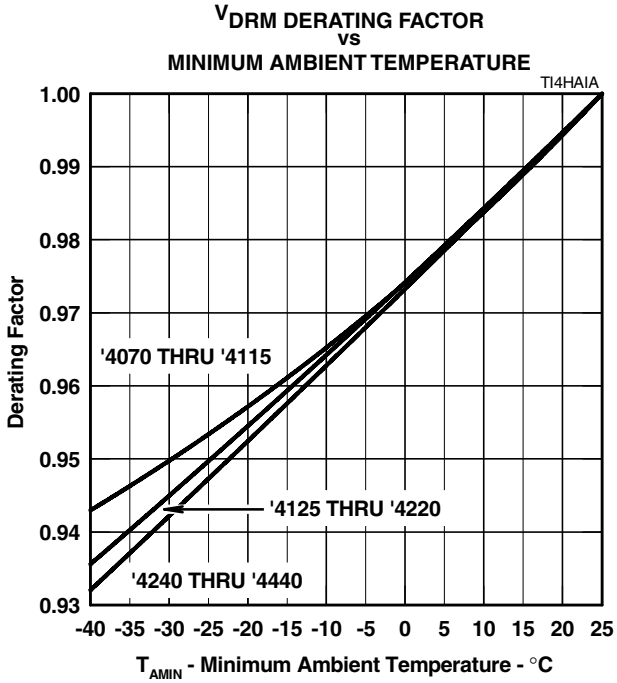

Figure 10.

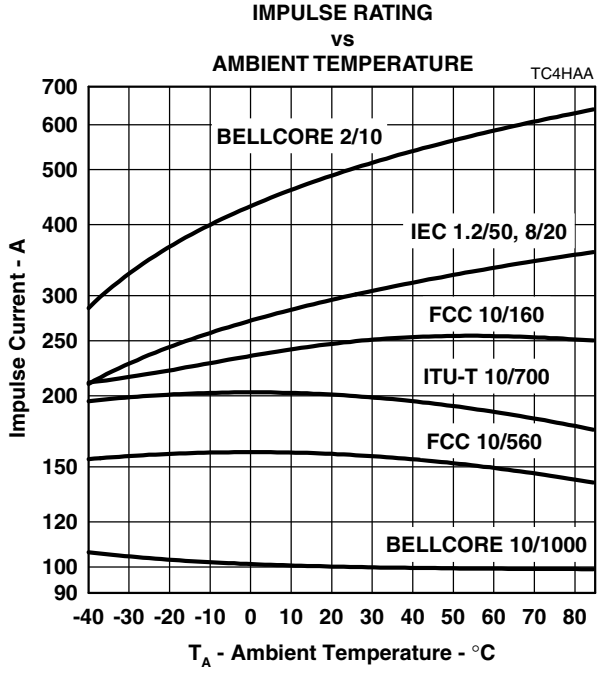

Figure 11.

APPLICATIONS INFORMATION

Deployment

These devices are two terminal overvoltage protectors. They may be used either singly to limit the voltage between two conductors (Figure 12) or in multiples to limit the voltage at several points in a circuit (Figure 13).

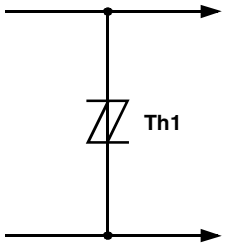

Figure 12. TWO POINT PROTECTION

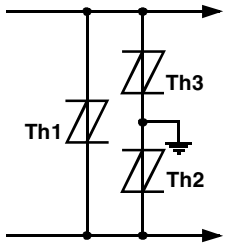

Figure 13. MULTI-POINT PROTECTION

In Figure 12, protector Th1 limits the maximum voltage between the two conductors to $\pm V_{(BO)}$. This configuration is normally used to protect circuits without a ground reference, such as modems. In Figure 13, protectors Th2 and Th3 limit the maximum voltage between each conductor and ground to the $\pm V_{(BO)}$ of the individual protector. Protector Th1 limits the maximum voltage between the two conductors to its $\pm V_{(BO)}$ value. If the equipment being protected has all its vulnerable components connected between the conductors and ground, then protector Th1 is not required.

Impulse Testing

To verify the withstand capability and safety of the equipment, standards require that the equipment is tested with various impulse wave forms. The table below shows some common values.

Standard	Peak Voltage Setting V	Voltage Waveform µs	Peak Current Value A	Current Waveform µs	TISP4xxxH3 25 °C Rating A	Series Resistance Ω
GR-1089-CORE	2500	2/10	500	2/10	500	0
	1000	10/1000	100	10/1000	100	
FCC Part 68 (March 1998)	1500	10/160	200	10/160	250	0
	800	10/560	100	10/560	160	0
	1500	9/720 †	37.5	5/320 †	200	0
	1000	9/720 †	25	5/320 †	200	0
I3124	1500	0.5/700	37.5	0.2/310	200	0
ITU-T K.20/K21	1500 4000	10/700	37.5 100	5/310	200	0

† FCC Part 68 terminology for the waveforms produced by the ITU-T recommendation K.21 10/700 impulse generator

If the impulse generator current exceeds the protector's current rating, then a series resistance can be used to reduce the current to the protector's rated value to prevent possible failure. The required value of series resistance for a given waveform is given by the following calculations. First, the minimum total circuit impedance is found by dividing the impulse generator's peak voltage by the protector's rated current. The impulse generator's fictive impedance (generator's peak voltage divided by peak short circuit current) is then subtracted from the minimum total circuit impedance to give the required value of series resistance. In some cases, the equipment will require verification over a temperature range. By using the rated waveform values from Figure 11, the appropriate series resistor value can be calculated for ambient temperatures in the range of -40 °C to 85 °C.

AC Power Testing

The protector can withstand currents applied for times not exceeding those shown in Figure 8. Currents that exceed these times must be terminated or reduced to avoid protector failure. Fuses, PTC (Positive Temperature Coefficient) resistors and fusible resistors are overcurrent protection devices which can be used to reduce the current flow. Protective fuses may range from a few hundred milliamperes to one ampere. In some cases, it may be necessary to add some extra series resistance to prevent the fuse opening during impulse testing. The current versus time characteristic of the overcurrent protector must be below the line shown in Figure 8. In some cases, there may be a further time limit imposed by the test standard (e.g. UL 1459 wiring simulator failure).

APPLICATIONS INFORMATION

Capacitance

The protector characteristic off-state capacitance values are given for d.c. bias voltage, V_D, values of 0, -1 V, -2 V and -50 V. Where possible, values are also given for -100 V. Values for other voltages may be calculated by multiplying the V_D = 0 capacitance value by the factor given in Figure 6. Up to 10 MHz, the capacitance is essentially independent of frequency. Above 10 MHz, the effective capacitance is strongly dependent on connection inductance. In many applications, such as Figure 15 and Figure 17, the typical conductor bias voltages will be about -2 V and -50 V. Figure 7 shows the differential (line unbalance) capacitance caused by biasing one protector at -2 V and the other at -50 V.

Normal System Voltage Levels

The protector should not clip or limit the voltages that occur in normal system operation. For unusual conditions, such as ringing without the line connected, some degree of clipping is permissible. Under this condition, about 10 V of clipping is normally possible without activating the ring trip circuit.

Figure 10 allows the calculation of the protector V_{DRM} value at temperatures below 25 °C. The calculated value should not be less than the maximum normal system voltages. The TISP4260H3LM, with a V_{DRM} of 200 V, can be used for the protection of ring generators producing 100 V rms of ring on a battery voltage of -58 V (Th2 and Th3 in Figure 17). The peak ring voltage will be 58 + 1.414*100 = 199.4 V. However, this is the open circuit voltage and the connection of the line and its equipment will reduce the peak voltage. In the extreme case of an unconnected line, clipping the peak voltage to 190 V should not activate the ring trip. This level of clipping would occur at the temperature when the V_{DRM} has reduced to 190/200 = 0.95 of its 25 °C value. Figure 10 shows that this condition will occur at an ambient temperature of -22 °C. In this example, the TISP4260H3LM will allow normal equipment operation provided that the minimum expected ambient temperature does not fall below -22 °C.

JESD51 Thermal Measurement Method

To standardize thermal measurements, the EIA (Electronic Industries Alliance) has created the JESD51 standard. Part 2 of the standard (JESD51-2, 1995) describes the test environment. This is a 0.0283 m^3 (1 ft^3) cube which contains the test PCB (Printed Circuit Board) horizontally mounted at the center. Part 3 of the standard (JESD51-3, 1996) defines two test PCBs for surface mount components; one for packages smaller than 27 mm (1.06 ”) on a side and the other for packages up to 48 mm (1.89 ”). The LM package measurements used the smaller 76.2 mm x 114.3 mm (3.0 ” x 4.5 ”) PCB. The JESD51-3 PCBs are designed to have low effective thermal conductivity (high thermal resistance) and represent a worse case condition. The PCBs used in the majority of applications will achieve lower values of thermal resistance and so can dissipate higher power levels than indicated by the JESD51 values.

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Typical Circuits

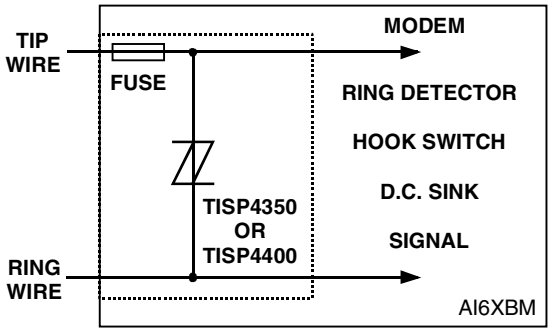


Figure 14. MODEM INTER-WIRE PROTECTION

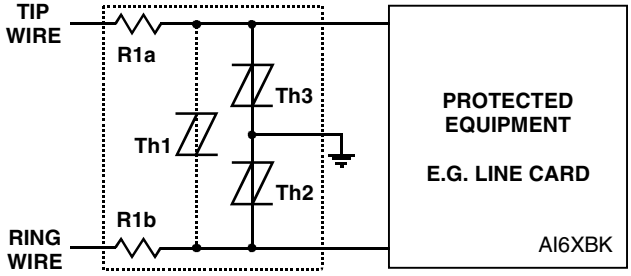


Figure 15. PROTECTION MODULE

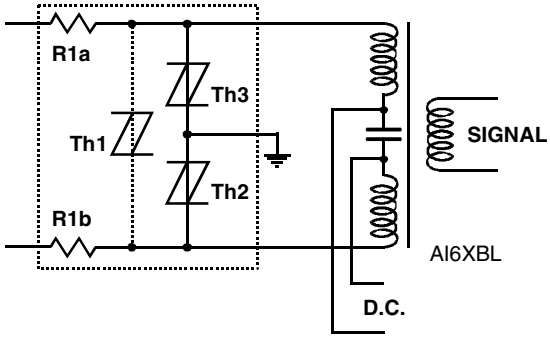


Figure 16. ISDN PROTECTION

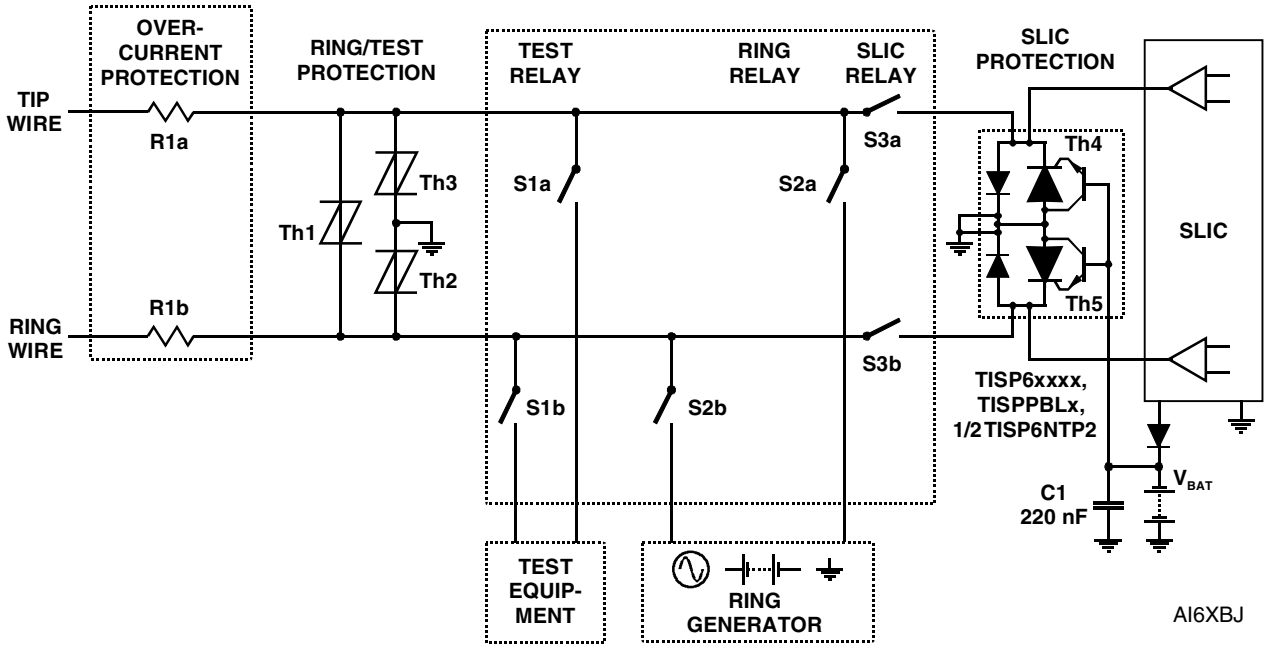


Figure 17. LINE CARD RING/TEST PROTECTION

MECHANICAL DATA

Device Symbolization Code

Devices will be coded as below.

Device	Symbolization Code
TISP4070H3LM	4070H3
TISP4080H3LM	4080H3
TISP4095H3LM	4095H3
TISP4115H3LM	4115H3
TISP4125H3LM	4125H3
TISP4145H3LM	4145H3
TISP4165H3LM	4165H3
TISP4180H3LM	4180H3
TISP4220H3LM	4220H3
TISP4240H3LM	4240H3
TISP4250H3LM	4250H3
TISP4260H3LM	4260H3
TISP4290H3LM	4290H3
TISP4300H3LM	4300H3
TISP4350H3LM	4350H3
TISP4395H3LM	4395H3
TISP4400H3LM	4400H3

Carrier Information

Devices are shipped in one of the carriers below. A reel contains 2,000 devices.

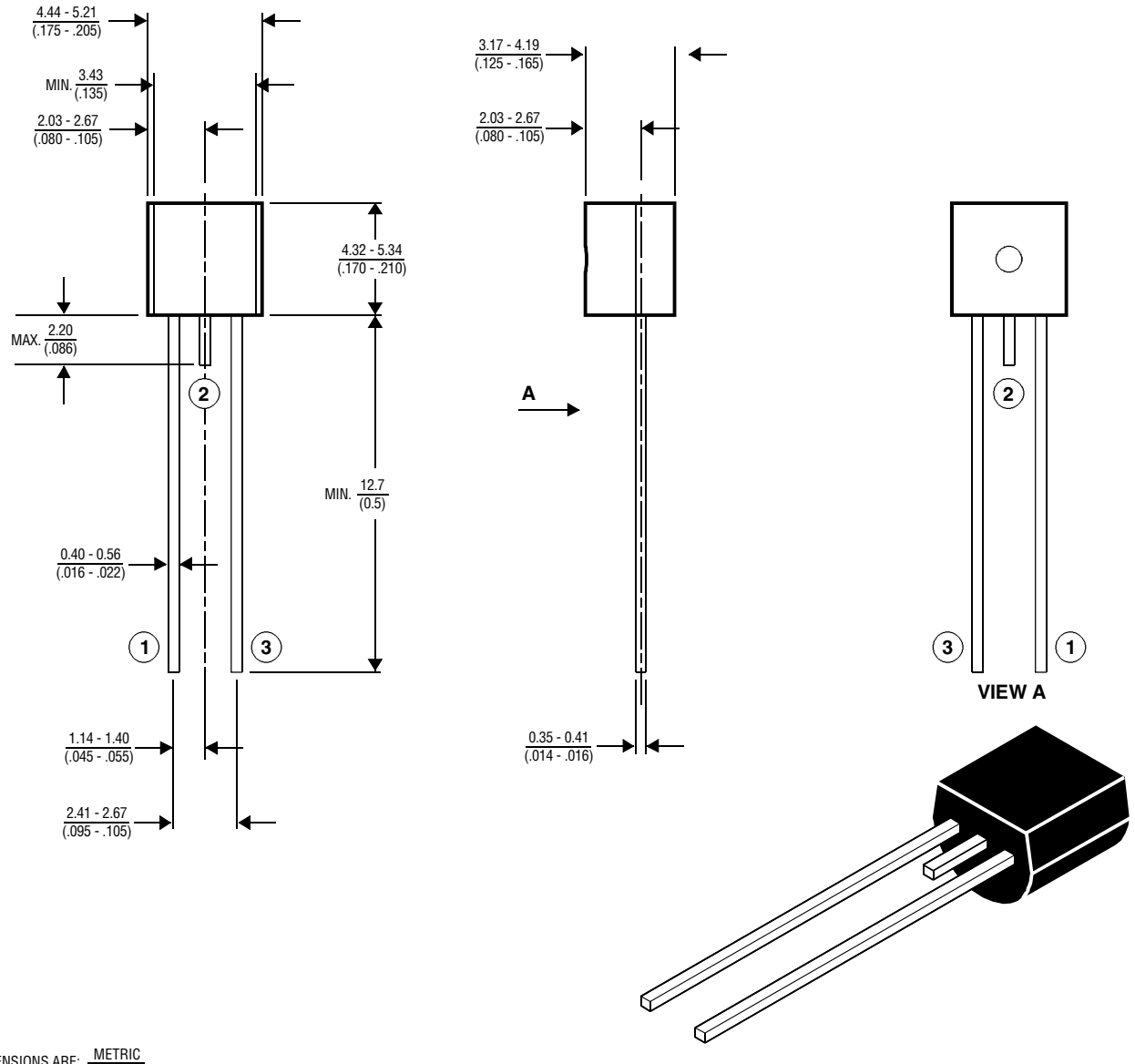
Package Type	Carrier	Order #
Straight Lead DO-92	Bulk Pack	TISP4xxxH3LM
Straight Lead DO-92	Tape and Reeled	TISP4xxxH3LMR
Formed Lead DO-92	Tape and Reeled	TISP4xxxH3LMFR

MECHANICAL DATA

LM002 (DO-92) 2-Pin Cylindrical Plastic Package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

LM002 Package (DO-92)



DIMENSIONS ARE: METRIC (INCHES)

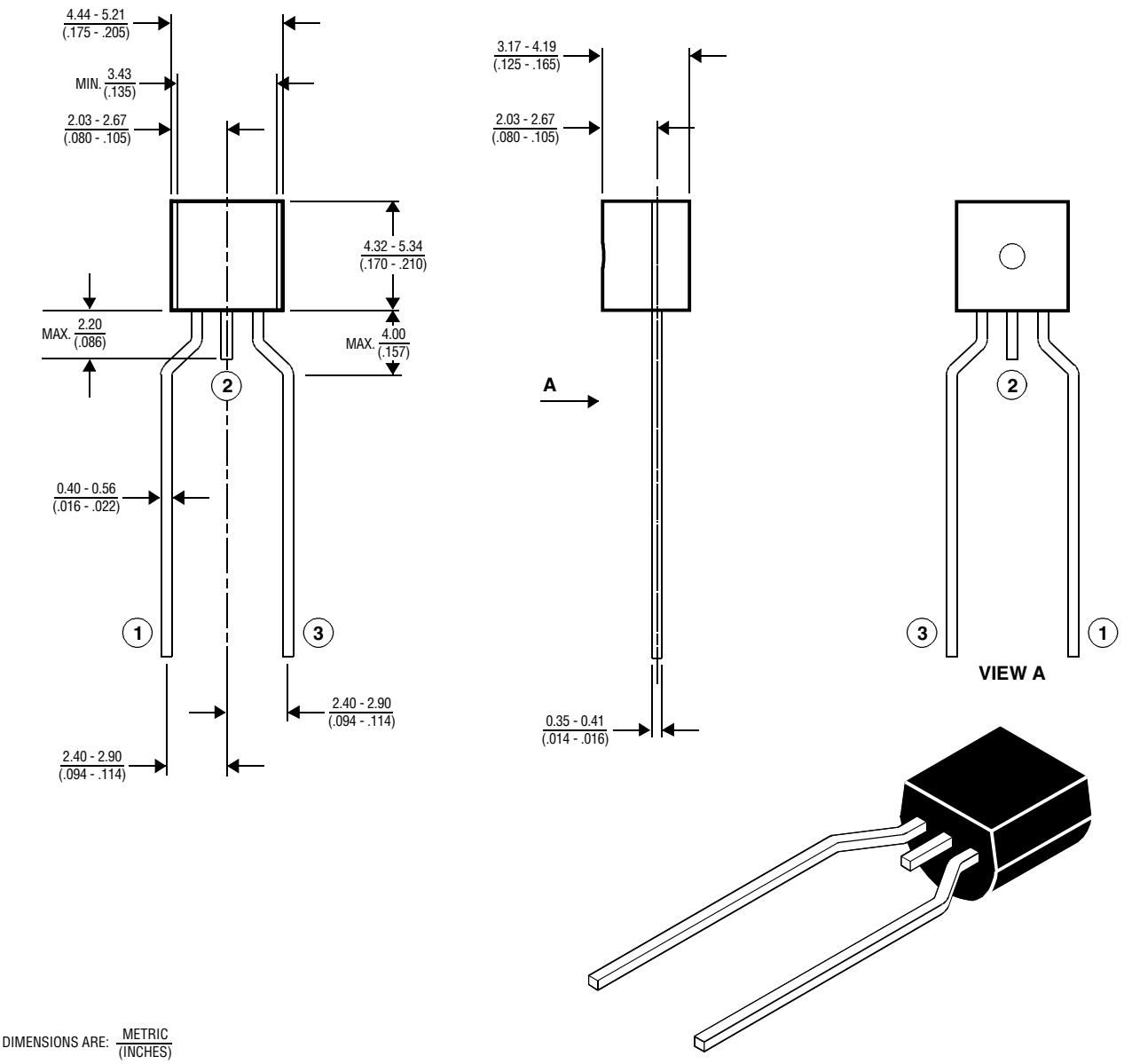
MD4XARA

MECHANICAL DATA

LM002 (DO-92) - Formed Leads Version 2-Pin Cylindrical Plastic Package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

LMF002 (DO-92) - Formed Leads Version of LM002



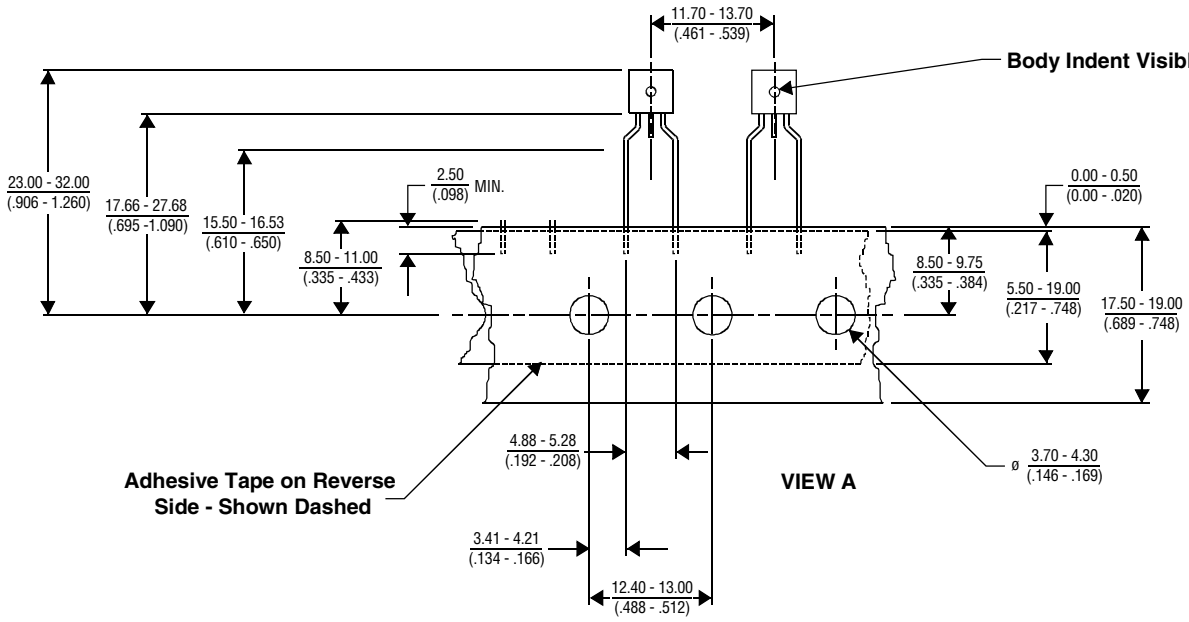
MD4XASA

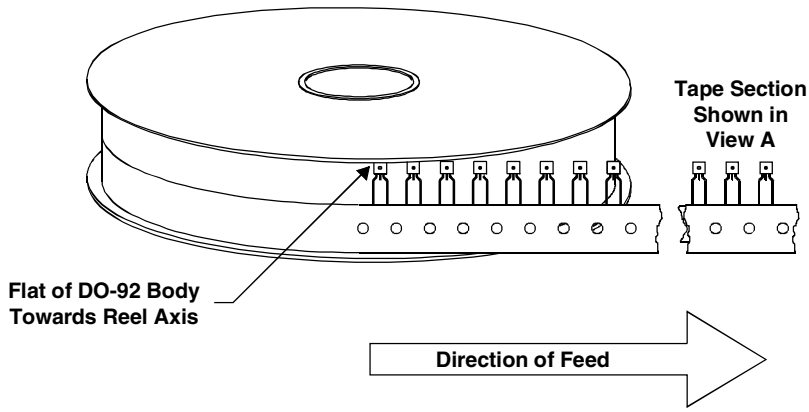
MECHANICAL DATA

Tape Dimensions

LMF002 Package (Formed Lead DO-92) Tape

LMF002 Tape Dimensions Conform to the Requirements of EIA-468-B





DIMENSIONS ARE: METRIC / (INCHES)

MD4XAQC